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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/914,077

08/23/2001

Satoshi Kawamura

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8442

2292

7590

06/05/2002

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EXAMINER

LEWIS, MONICA

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 06/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 09/914,077	Applicant(s) KAWAMURA ET AL.	
	Examiner Monica Lewis	Art Unit 2822	<i>Me</i>

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 22 April 2002.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-6 and 9-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6 and 9-19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 August 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                  | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____  |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                         | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>3</u> . | 6) <input type="checkbox"/> Other: _____                                    |

### **DETAILED ACTION**

1. This office action is in response to the election filed April 22, 2002.

#### ***Election/Restrictions***

2. Applicant's election with traverse of an integrated circuit element with a coil on a chip in Paper No. 7 is acknowledged. The traversal is on the ground(s) that there is no burden for the examiner to examine both groups. This is not found persuasive because searching in a separate area for method (Class 438) and another area for apparatus (Class 257) for two inventions does constitute an undue burden upon the examiner.

The requirement is still deemed proper and is therefore made FINAL.

#### ***Drawings***

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because of the following: a) reference character "12" has been used to designate both circuit and photoresist layer (See Page 17 Lines 13 and 27); and b) reference character "116" has been used to designate both emitter polysilicon and film (See Page 8 Lines 1 and 17). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

#### ***Specification***

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.
5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

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6. The disclosure is objected to because of the following informalities: a) the headings are not correct for the specification.

Appropriate correction is required.

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

### **Arrangement of the Specification**

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

- (a) TITLE OF THE INVENTION.
- (b) CROSS-REFERENCE TO RELATED APPLICATIONS.
- (c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
- (d) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)
- (e) BACKGROUND OF THE INVENTION.
  - (1) Field of the Invention.
  - (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
- (f) BRIEF SUMMARY OF THE INVENTION.
- (g) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
- (h) DETAILED DESCRIPTION OF THE INVENTION.
- (i) CLAIM OR CLAIMS (commencing on a separate sheet).
- (j) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
- (k) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

***Claim Rejections - 35 USC § 102***

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 9, 11 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Droz (U.S. Patent No. 5,399,847).

In regards to claim 9, Droz discloses the following:

a) information carrier including a substrate (128) having mounted thereon an IC element (124) formed integrally with an antenna coil (108) for performing data communication in a contactless manner with external equipment, characterized in that said IC element is disposed at a center portion of said substrate in a planar direction perpendicularly to a plane of said substrate (See Figure 10).

In regards to claim 11, Droz discloses the following:

a) only one surface of said IC element is covered with said substrate (See Figure 11).

In regards to claim 12, Droz discloses the following:

a) substrate is formed in a circular or square planar shape (See Figure 10).

***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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10. Claims 1-6, 14 and 15 are rejected under 35 U.S.C. 103(a) as obvious over Droz et al. (U.S. Patent No. 5,399,847) in view of Shindo et al. (U.S. Patent No. 5,048,179).

In regards to claim 1, Droz discloses the following:

a) IC element (2) formed integrally with a coil for performing contactless data communication with external equipment, characterized in that a conductor constituting said coil is implemented in a multilayer structure (See Figures 6 and 7).

In regards to claim 1, Droz fails to disclose the following:

a) a metal-sputtered layer or alternatively a metal-evaporated layer and a metal plated layer.

However, the limitation of "metal-sputtered layer or alternatively a metal-evaporated layer and a metal plated layer" makes it a product by process claim. The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A "*product by process*" claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972); *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); *In re Fessmann*, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a "*product by, all of*" claim, and not the patentability of the process, and that an old or obvious product, whether

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claimed in "*product by process*" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

In regards to claim 2, Droz fails to disclose the following:

a) a metal-sputtered layer or alternatively a metal-evaporated layer and a metal plated layer.

However, the limitation of "metal-sputtered layer or alternatively a metal-evaporated layer and a metal plated layer" makes it a product by process claim. The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A "*product by process*" claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972); *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); *In re Fessmann*, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a "*product by, all of*" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "*product by process*" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

b) at least one metal of aluminum, nickel, copper and chromium or alternatively an alloy containing those metals.

However, Shindo et al. ("Shindo") discloses aluminum, copper and chromium (See Column 5 Lines 7-11). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Droz to include aluminum, copper and chromium as disclosed in Shindo because they aid in providing an electrical connection among the components.

In regards to claim 3, Droz discloses the following:

a) coil is formed on a surface of said IC element formed with input/output terminals (See Figure 6).

In regards to claim 3, Droz fails to disclose the following:

a) passivation film.

However, Shindo discloses a passivation layer (See Column 5 Lines 3-7). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Droz to include a passivation layer as disclosed in Shindo because it is utilized to prevent deterioration of electronic properties.

b) holes.

However, Shindo discloses the use of a via hole (See Column 3 Lines 61-67). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Droz to include a via hole as disclosed in Shindo because it provides a means for components to interconnect.

In regards to claim 4, Droz discloses the following:

a) coil is implemented in a rectangular spiral pattern in a planar shape and that all or some of corner portions of said rectangular spiral pattern are chamfered (See Figure 6).



In regards to claim 5, Droz fails to disclose the following:

a) metal-plated layer is formed by resorting to a electroless plating method or alternatively an electroplating method or alternatively a precision electroforming method.

However, the limitation of "electroless plating method or alternatively an electroplating method or alternatively a precision electroforming method" makes it a product by process claim. The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A "*product by process*" claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972); *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); *In re Fessmann*, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a "*product by, all of*" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "*product by process*" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

In regards to claim 6, Droz fails to disclose the following:

a) line width of said coil is not smaller than 7 um, an inter-line distance thereof is not greater than 5 um and the number of turns thereof is not smaller than 20 turns.

However, the applicant has not established the critical nature of the dimension of “7 um, an inter-line distance thereof is not greater than 5 um and the number of turns thereof is not smaller than 20 turns.” “The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.” *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

In regards to claim 14, Droz discloses the following:

a) a three-bonded-layer structure including a top member, a bottom member and an intermediate member (See Column 3 Lines 21-31).

In regards to claim 14, Droz fails to disclose the following:

a) IC element is accommodated within a through-hole formed in said intermediate member at a mid portion thereof.

However, Shindo discloses the use of a via hole (See Column 3 Lines 61-67). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Droz to include a via hole as disclosed in Shindo because it provides a means for components to interconnect.

In regards to claim 15, Droz fails to disclose the following:

a) though-hole is formed circularly in a planar shape.

However, Shindo discloses the use of a via hole (See Column 3 Lines 61-67). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Droz to include a via hole as disclosed in Shindo because it provides a means for components to interconnect.

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8. Claims 10 and 19 are rejected under 35 U.S.C. 103(a) as obvious over Droz et al. (U.S. Patent No. 5,399,847) in view of Masahiko (U.S. Patent No. 5,852,289).

In regards to claim 10, Droz fails to disclose the following:

a) top and bottom surfaces of said IC element are covered with said substrate.

However, Masahiko discloses top and bottom surfaces of an IC element (123) covered with substrate (122 and 121b) (See Figure 18). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Droz to include top and bottom surfaces of said IC element are covered with said substrate as disclosed in Masahiko because it provides a base for the device to be built upon.

In regards to claim 19, Droz fails to disclose the following:

a) discrete coil which is separately formed independent of said IC element internally of said substrate.

However, Masahiko discloses a coil (125) that is formed independent of the IC element (123) and internally of said substrate (121a, 121b and 122) (See Figure 16). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Droz to include top and bottom surfaces of said IC element are covered with said substrate as disclosed in Masahiko because it aids in increasing the power.

12. Claim 13 is rejected under 35 U.S.C. 103(a) as obvious over Droz et al. (U.S. Patent No. 5,399,847) in view of Parmentier (U.S. Patent No. 4,483,067).

In regards to claim 13, Droz fails to disclose the following:

a) substrate is wholly or partially formed of paper.

However, Parmentier discloses the use of a paper substrate (See Column 2 Lines 41-46). It would have been obvious to one having ordinary skill in the art at the time the invention was

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made to modify the semiconductor of Droz to include a paper substrate as disclosed in Parmentier because it provides a base for the device to be built upon.

13. Claims 16-18 are rejected under 35 U.S.C. 103(a) as obvious over Droz et al. (U.S. Patent No. 5,399,847) in view of Fidalgo (U.S. Patent No. 5,598,032).

In regards to claim 16, Droz discloses the following:

a) substrate is implemented in a two-bonded-layer structure including a top member and a bottom member (See Column 3 Lines 21-31).

In regards to claim 16, Droz fails to disclose the following:

a) IC element is accommodated within a recess formed in said top member or alternatively in said bottom member at a mid portion thereof.

However, Fidalgo discloses a chip placed in a recess (See Column 5 Lines 31-50). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Droz to include a chip placed in a recess as disclosed in Fidalgo because it provides a means for components to interconnect.

In regards to claim 17, Droz discloses the following:

a) substrate is implemented in a single layer structure (See Column 2 Lines 62-68 and Column 3 Lines 1-2).

In regards to claim 17, Droz fails to disclose the following:

a) IC element is accommodated within a recess formed in said substrate at a mid portion thereof.

However, Fidalgo discloses a chip placed in a recess (See Column 5 Lines 31-50). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Droz to include a chip placed in a recess as disclosed in Fidalgo because it provides a means for components to interconnect.

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In regards to claim 18, Droz fails to disclose the following:

a) recess is formed circularly in a plane shape.


However, Fidalgo discloses a recess that can have different shapes (See Column 5 Lines 34-35). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Droz to include a recess that can have different shapes as disclosed in Fidalgo because it provides a means for components to interconnect.

### ***Conclusion***

15. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: a) Takahira (U.S. Patent No. 5,424,527) discloses a non-contact type ic card; and b) Onozawa (U.S. Patent No. 5,837,992) discloses a memory card.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 703-308-4940. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML  
May 31, 2002

  
**CARL WHITEHEAD, JR.**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2800**